AFE – DFE hardware chain
DØ Interface

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FPD DFE – Data Pump Test
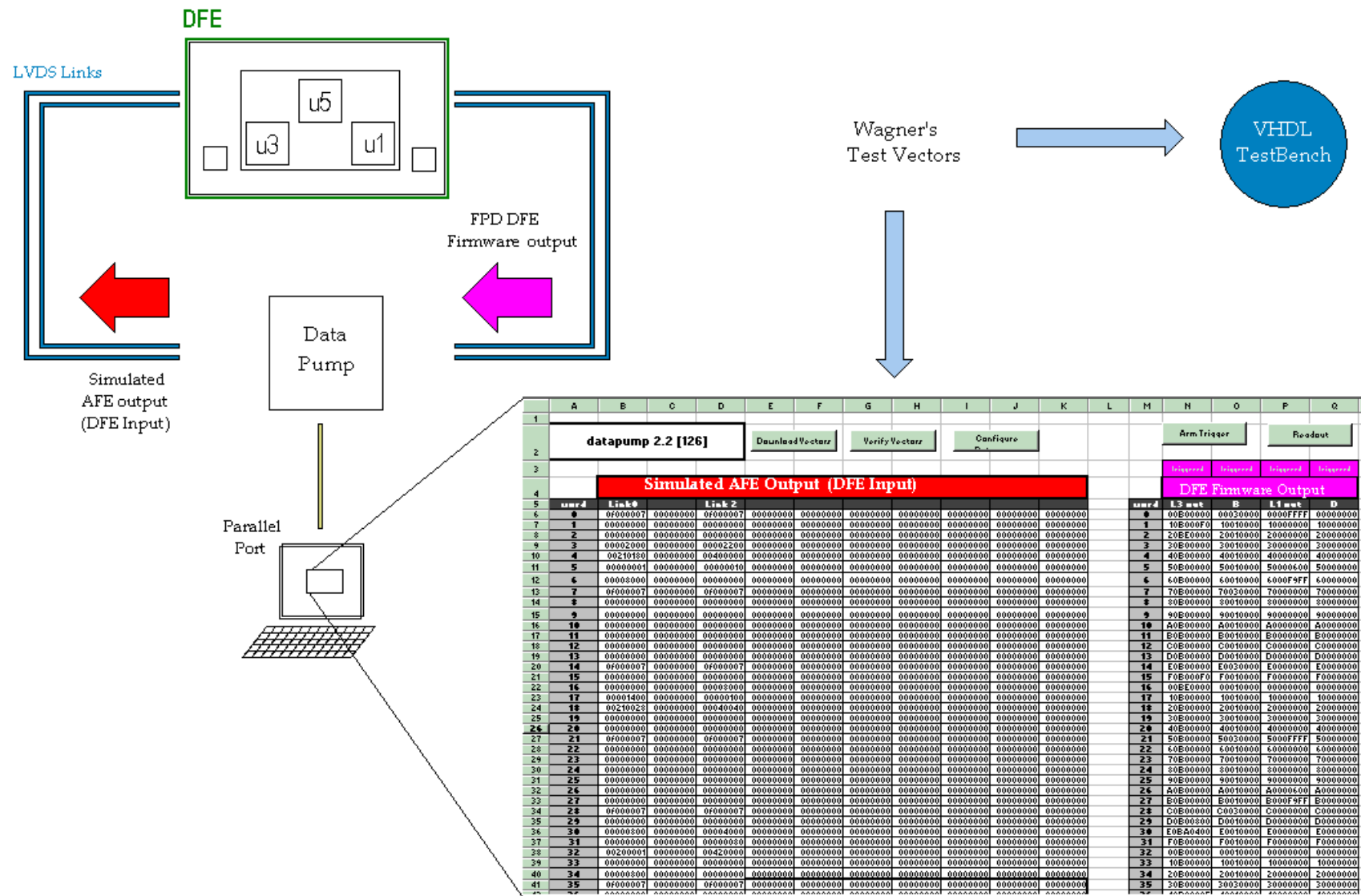
FPD firmware – VHDL Test Bench
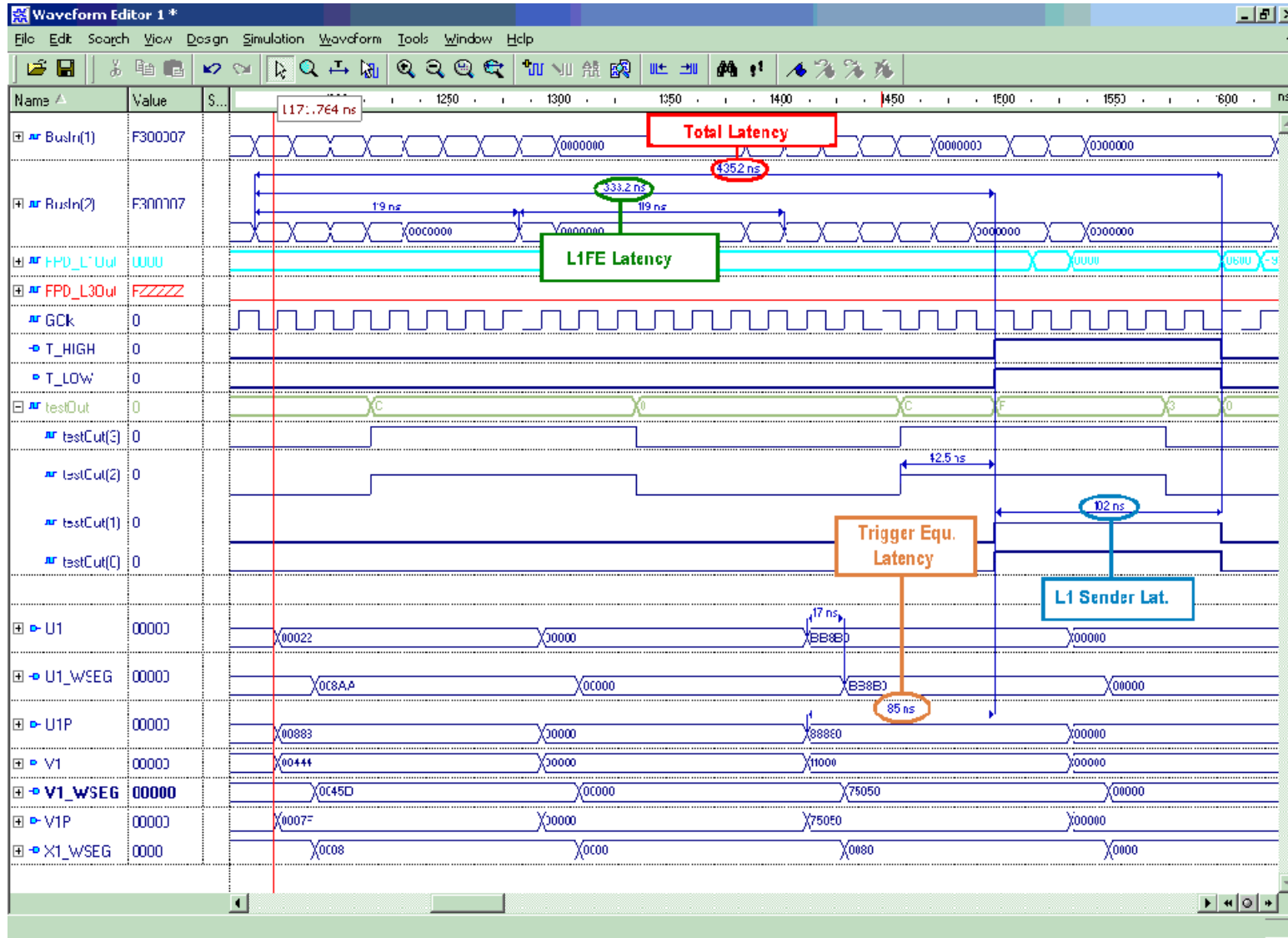
FPD firmware – Implementation

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Timing summary:
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Timing errors: 3   Score: 438

Constraints cover 24579 paths, 3 nets, and 12117 connections (97.9% coverage)

Design statistics:
    Minimum period:  14.299ns (Maximum frequency:  69.935MHz)
    Minimum input arrival time before clock:    2.100ns
    Minimum output required time after clock:    7.190ns


Analysis completed Wed Feb 19 09:45:24 2003
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Design Summary:
    Number of errors:       0
    Number of warnings:     9
    Number of Slices:              1,709 out of  6,912    24%
    Number of Slices containing
        unrelated logic:               0 out of  1,709     0%
    Number of Slice Flip Flops:      855 out of 13,824     6%
    Total Number 4 input LUTs:     3,139 out of 13,824    22%
        Number used as LUTs:                     3,115
        Number used as a route-thru:                16
        Number used as Shift registers:              8
    Number of bonded IOBs:           109 out of    404    26%
        IOB Flip Flops:                            115
    Number of Block RAMs:              4 out of     72     5%
    Number of GCLKs:                   3 out of      4    75%
    Number of GCLKIOBs:                3 out of      4    75%
Total equivalent gate count for design:  93,349
Additional JTAG gate count for IOBs:  5,376
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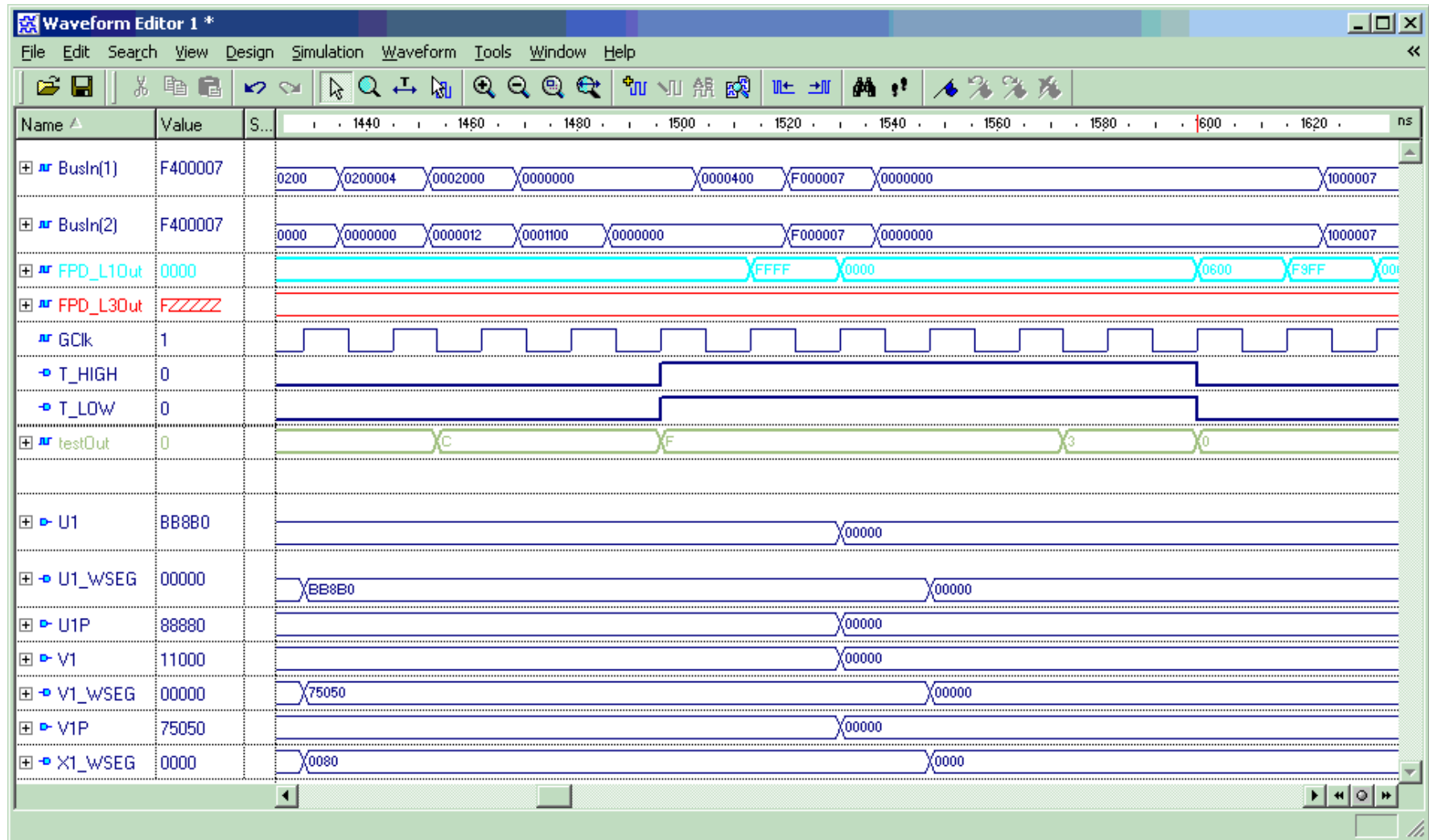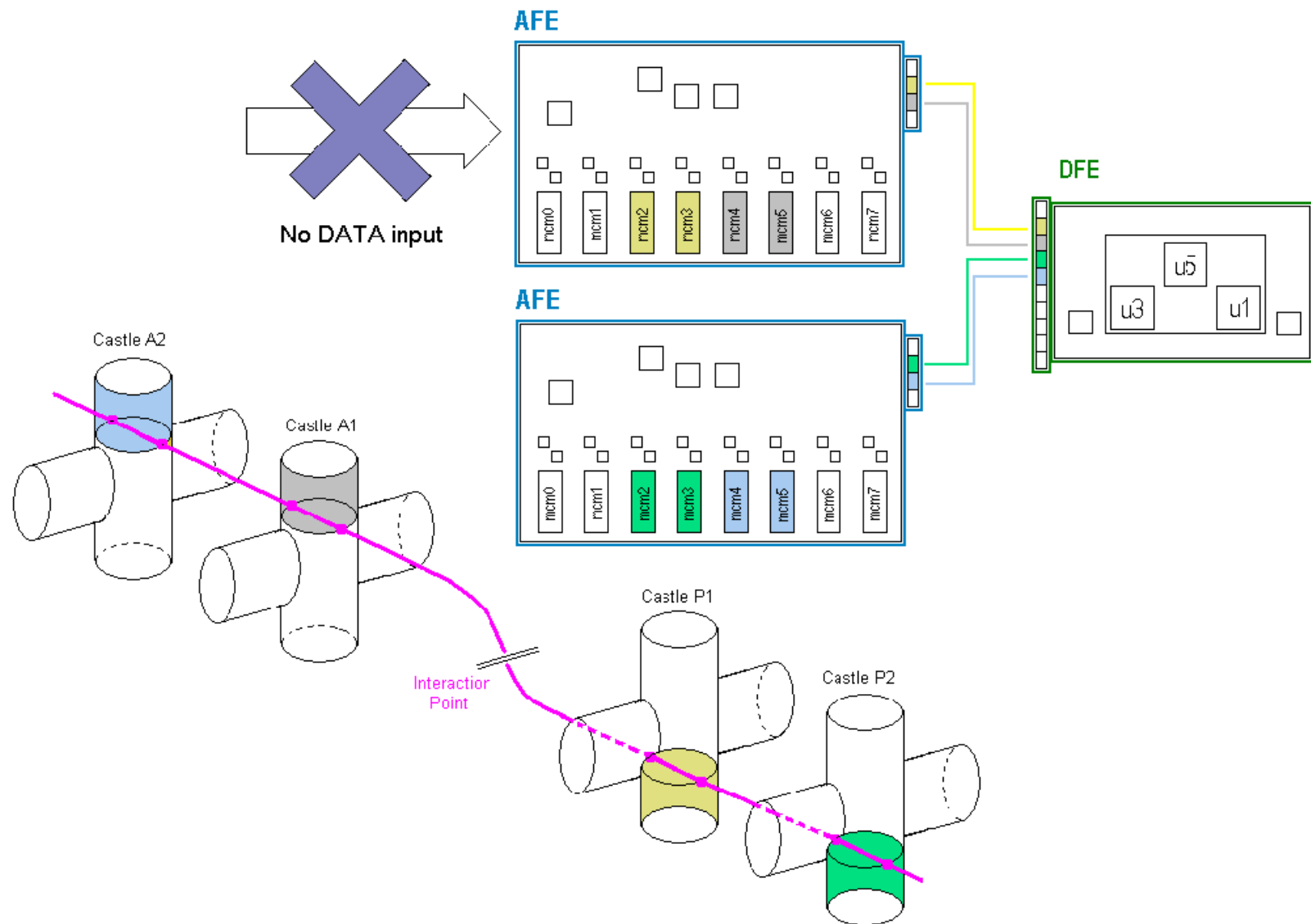
Trigger Equations – Output

Trigger Chain – Personality Code